



Reference Specification

Chip Monolithic Ceramic Capacitor specific application

(GR4 Series X7R Char. Test Voltage DC3kV)

Product specifications in this drawing are subject to change or our products described in this drawing may be discontinued without advance notice.

The parts numbers and specifications listed in this drawing are for information only. You are requested to transact the "Product Specification", before your ordering.

Product Engineering Section High Voltage Capacitor Group Izumo Murata Manufacturing Co., Ltd.

		Kele	rence only		
A					
1.0PERATING				h (
					ain the Vp-p value of the
					he voltage is started to
		e to use a capacitor w			ansit period because of
					(AC filter), be sure to use
					e withstand established for
each equipm	ent should be take	en into considerations		voltage of impulse	
Voltage	DC Voltage	DC+AC Voltage	AC Voltage	Pulse Voltage(1) Pulse Voltage(2)
Voltago					
Positional	Vo-p		Vp-p	Vp-p	Vp-p
Measurement					
	<u> </u>				
	<u> </u>		· ·		
2.0PERATING	TEMPERATURE	AND SELF-GENERA	TED HEAT		
	-			rated operating te	mperature range. Be sur
		enerated by the capa			
					s. Applied voltage should
		heat is within 20°C c			
					dition where capacitor is
					t may lead to deterioratio
					th the cooling fan running
		nent cannot be ensure			
		ITHSTANDING VOLT	,		
(1)TEST EQUI					
		ding voltage shall be	used with the perfor	mance of the way	e similar to 50/60 Hz sin
					ied, the defective may be
caused.			5 • • • • •		, ,
(2)VOLTAGE A	APPLIED METHO	C			
			s lead or terminal sh	all be firmly conne	ected to the out-put of th
					to the test voltage. If the
					r, test voltage should be
					to near zero, and then
		all be taken off the out			
					e surge voltage may arise
	e, the defective ma				
*ZERO CI	ROSS is the point	where voltage sine wa	ave pass 0V.		voltage sine wave
- See the	e right figure -				
				0)/	
				0V	
					zero cross
4.FAIL-SAFE					
-	itor would be brok	on failuro may result	in a short circuit Be	sure to provide a	in appropriate fail-safe
		oduct if failure would for			in appropriate rail-sale
TUTICUOTTIKE	a luse on your pro		bliow an electric sho	ock, me or fume.	
5. VIBRATION					
	-	s leads to excessive s	bock or vibration du		
Do not expos				ining use.	
	JT FOR CROPPIN				
			d on the chin during	flowing or bonding	of the beard
		at minimizes imposed			
[Component d	nection]			iounting Close to	Board Separation Point]
	1.	Locate chip hor			
	Di Ta	the direction in	which Perfo	ration	Chip arrangement Worst A>C>B~D Best
/ 🖽 🌙	\$ <i>™</i> ->/ <i>⊟</i> /	stress acts.			WOIST AND AD BEST
		i = 1 ^{''V}			
				A slit	
	OARD MATERIAL			\sim	
		citor is soldered on the	e metal hoard, such	as Aluminum boo	ind the stress of host
					ce of thermal expansion
		d and ceramic chip.	coramic capacitor, c		
	ween metal poar	and ceramic chip.			
G07G					

8. SOLDERING

- 8-1. Reflow Soldering(1) When the sudden heat is given to the components, the mechanical strength of the components should go down because remarkable temperature change causes deformity of components inside. In order to prevent mechanical damage in the components, preheating should be required for both of the components and the PCB board. Preheating conditions are shown in table 1. It is required to keep temperature differential between the soldering and the components surface (ΔT) as small as possible.
- (2) Solderability of Tin plating termination chip might be deteriorated when low temperature soldering profile where peak solder temperature is below the Tin melting point is used. Please confirm the solderability of Tin plating termination chip before use.
- (3) When components are immersed in solvent after mounting, be sure to maintain the temperature difference (ΔT) between the component and solvent within the range shown in the table 1.

Table 1

Part Number	Temperature Differential
G 🗆 🗆 18/21/31	$\Delta T \leq 190^{\circ}C$
G 🗆 🗆 32/42/43/52/55	$\Delta T \leq 130^{\circ}C$

Recommended Conditions

	Pb-Sn S	Lead Free	
	Infrared Vapor Reflow Reflow		Solder
Peak Temperature	230-250°C	230-240°C	240-260°C
Atmosphere	Air	Air	Air or N2

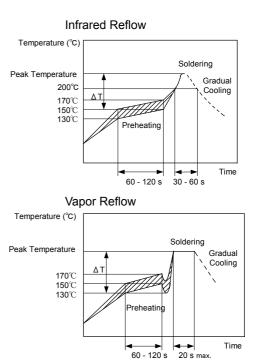
Pb-Sn Solder : Sn-37Pb

Lead Free Solder : Sn-3.0Ag-0.5Cu

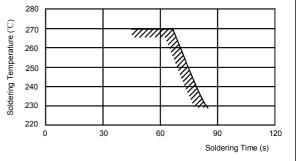
- (4) Optimum Solder Amount for Reflow Soldering Overly thick application of solder paste results in excesive fillet height solder. This makes the chip more susceptible to
 - mechanical and thermal stress on the board and may cause cracked chips.
 - Too little solder paste results in a lack of adhesive strength on the outer electrode, which may result in chips breaking loose from the PCB.
 - Make sure the solder has been applied smoothly to the end surface to a height of 0.2mm min

Inverting the PCB Make sure not to impose an abnormal mechanical shock on the PCB.

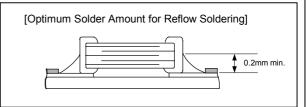
[Standard Conditions for Reflow Soldering]



[Allowable Soldering Temperature and Time]



In case of repeated soldering, the accumulated soldering time must be within the range shown above.



8-2. Flow Soldering

- (1) When the sudden heat is given to the components, the mechanical strength of the components should go down because remarkable temperature change causes deformity of components inside. And an excessively long soldering time or high soldering temperature results in leaching of the outer electrodes, causing poor adhesion or a reduction in capacitance value due to loss of contact between electrodes and end termination.
- (2) In order to prevent mechanical damage in the components, preheating should be required for both of the components and the PCB board.

Preheating conditions are shown in table 2. It is required to keep temperature differential between soldering and the components surface (ΔT) as small as possible. When components are immersed in solvent after mounting, be sure to maintain the temperature difference between the component and solvent within the range shown in Table 2.

Do not apply flow soldering to chips not listed in Table 2.

Table 2

Part Number	Temperature Differential
G□□18/21/31	∆T≦150°C

Recommended Conditions

	Pb-Sn Solder	Lead Free Solder
Peak Temperature	240-250°C	250-260°C
Atmosphere	Air	N2

Pb-Sn Solder : Sn-37Pb

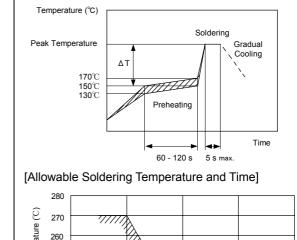
Lead Free Solder : Sn-3.0Ag-0.5Cu

(3) Optimum Solder Amount for Flow Soldering

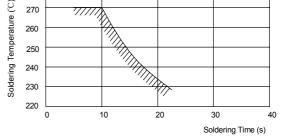
Please refer to right figure.

The top of the solder fillet should be lower than the thickness of components. If the solder amount is excessively big, the risk of cracking is higher during board bending or under any other stressful conditions.

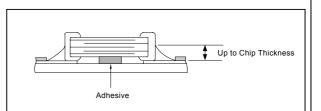
8-3. Correction with a Soldering Iron



[Standard Conditions for Flow Soldering]



In case of repeated soldering, the accumulated soldering time must be within the range shown above.



(1) When sudden heat is applied to the components by use of a soldering iron, the mechanical strength of the components will go down because the extreme temperature change causes deformations inside the components. In order to prevent mechanical damage to the components, preheating is required for both the components and the PCB board. Preheating conditions, (The "Temperature of the Soldering Iron tip", "Preheating Temperature", "Temperature Differential" between iron tip and the components and the PCB), should be within the conditions of table 3. It is required to keep the temperature differential between the soldering Iron and the components surface (ΔT) as small as possible. After soldering, do not allow the component/PCB to cool down rapidly. The operating time for the re-working should be as short as possible. When re-working time is too long, it may cause solder leaching, and that will cause a reduction of the adhesive strength of the terminations.

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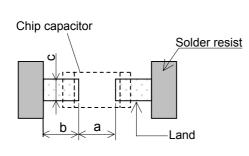
Part Number	Temperature of Soldering Iron tip	Preheating Temperature	Temperature Differential (ΔT)	Atmosphere
G□□18/21/31	350°C max.	150°C min.	∆T≦190°C	air
G□□32/42/43/52/55	280°C max.	150°C min.	∆T≦130°C	air
Pb-Sn Solder : Sn-37Pb Lead Free Solder : Sn-3.0Ag (2) Optimum Solder Amoun In case of smaller sizes solder fillet should be low of the component or 0.5 In case of larger sizes ti fillet should be lower tha component. If the solde cracking is higher during stressful conditions. Sol φ 3mm or smaller shou keep the soldering iron during the re-work. Sold is required for soldering Do not touch the chip capace the ion ingredient brought fr OPERATING AND STORAC Do not use or store capacito or the like are present. And a these processes do not affer the intended equipment. Sto and 20 to 70%. Use capacite ailure to follow the above car LIMITATION OF APPLICATI Please contact us before us for the prevention of defects (1) Aircraft equipment (4) Power plant control d (6) Transportation equip (7) Traffic signal equipm (9) Data-processing equ (10) Application of simila	t when re-working Usi than G \square 18, the top wer than 2/3's of the t imm whichever is sma han G \square 21, the top an 2/3's of the thickness r amount is excessive g board bending or un dering iron ld be used. It is also n from touching the corr ler wire with ϕ 0.5mm ler wire with ϕ 0.5mm between the correlation on human finger or has GE ENVIROMENT rs in a corrosive atmost avoid exposure to mois avoid exposur	p of the hickness aller. of the solder ss of the , the risk of der any other ecessary to ponents or smaller c body directly. The s and. sphere, especially wi sture. Before cleaning esting the performan re the temperature a ter delivered. Check st case, in a short cin the applications listed cause damage to the ospace equipment dical equipment , ships, etc.) saster prevention/crin	here chloride gas, sul ng, bonding or molding ce of a cleaned, bonc and relative humidity of the solderability in ca rcuit and fuming wher below which require third party's life, bod (3) Undersea me prevention equipn	fide gas, acid, alkali, sa g this product, verify th led or molded product do not exceed 5 to 40° se of 6 months or mor n the product is used. especially high reliabili y or property. a equipment nent

♦ NOTICE

1.CONSTRUCTION OF BOARD PATTERN

After installing chips, if solder is excessively applied to the circuit board, mechanical stress will cause destruction resistance characteristics to lower. To prevent this, be extremely careful in determining shape and dimension before designing the circuit board diagram.

1-1.Construction and dimensions of pattern (example)

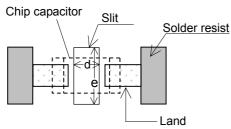


 Reflow soldering 			
$(L \times W)$	а	b	С
1.6 × 0.8	0.6 to 0.8	0.6 to 0.7	0.6 to 0.8
2.0 × 1.25	1.0 to 1.2	0.6 to 0.7	0.8 to 1.1
3.2 × 1.6	2.2 to 2.4	0.8 to 0.9	1.0 to 1.4
3.2 × 2.5	2.0 to 2.4	1.0 to 1.2	1.8 to 2.3
4.5 imes 2.0	2.8 to 3.4	1.2 to 1.4	1.4 to 1.8
4.5 × 3.2	2.8 to 3.4	1.2 to 1.4	2.3 to 3.0
5.7 × 2.8	4.0 to 4.6	1.4 to 1.6	2.1 to 2.6
5.7 × 5.0	4.0 to 4.6	1.4 to 1.6	3.5 to 4.8

Flow soldering

*Flow soldering : 3.2×1.6 or less	$(L \times W)$	а	b	С
	1.6 × 0.8	0.6 to 1.0	0.8 to 0.9	0.6 to 0.8
available.	2.0 × 1.25	1.0 to 1.2	0.9 to 1.0	0.8 to 1.1
	3.2 × 1.6	2.2 to 2.6	1.0 to 1.1	1.0 to 1.4

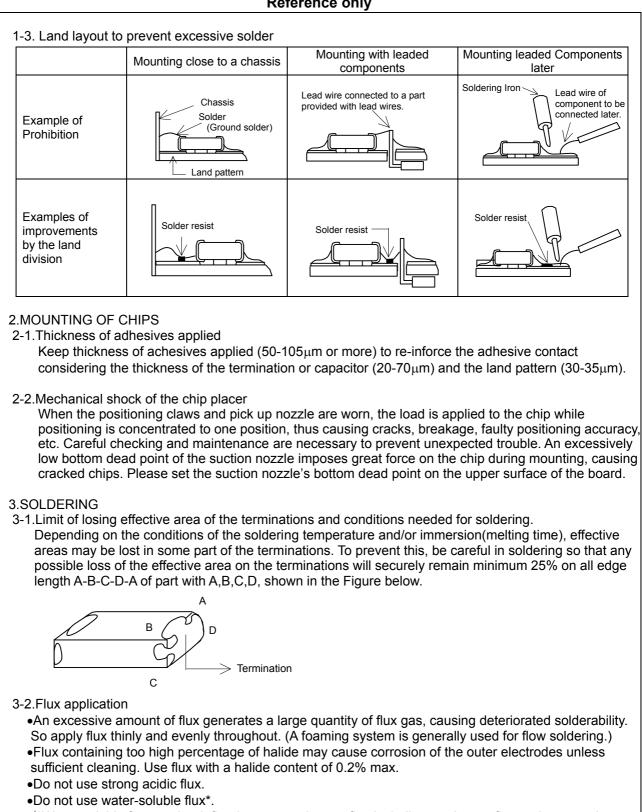
1-2. Dimension of slit (example)



	$(L \times W)$	d	е
	1.6 × 0.8	-	-
st	2.0 × 1.25	-	-
<u>51</u>	3.2 × 1.6	1.0 to 2.0	3.2 to 3.7
	3.2 × 2.5	1.0 to 2.0	4.1 to 4.6
	4.5 × 2.0	1.0 to 2.8	3.6 to 4.1
	4.5 × 3.2	1.0 to 2.8	4.8 to 5.3
	5.7 × 2.8	1.0 to 4.0	4.4 to 4.9
	5.7 × 5.0	1.0 to 4.0	6.6 to 7.1

*Preparing slit help flux cleaning and resin coating on the back of the capacitor. But, the length of slit design should be shorter enough as much as possible to prevent the mechanical damage in the capacitor.

The longer slit design might receive more severe mechanical stress from the PCB. Recommendable slit design is shown in the Table.



(*Water-soluble flux can be defined as non rosin type flux including wash-type flux and non-wash-type flux.)

4.CLEANING

Please confirm there is no problem in the reliability of the product beforehand when cleaning it with a intended equipment. The residual substance after cleaning might cause the decrease in the surface resistance of the chip and the corrosion of the electrode part, etc. As a result might cause reliability to deteriorate.

Please confirm there is not problem with a intended equipment in the ultrasonic cleansing beforehand.

5.ROSIN COATING

Please use it after confirming there is no influence on the product with a intended equipment beforehand rosin coating or molding. The chip crack might be caused at the thermal unever thickness of the rosin.

When selecting rosin materials, select those with low contraction and low moisture absorption coefficient (generally epoxy rosin is used).

6.CAPACITANCE CHANGE OF CAPACITOR

The capacitor specified in this product specification have an aging characteristic, whereby the capacitor continually decreases its capacitance slightly if the capacitor leaves for a long time. Moreover, capacitance might change greatly depending on a surrounding temperature or an applied voltage. So, it is not likely to be able to use for the time constant circuit. Please contact us if you need a detail information.

▲NOTE

1.Please make sure that your product has been evaluated in view of your specifications with our product being mounted to your product.

2. You are requested not to use our product deviating from this specification.

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Telecommunication of DC-DC Converte	devices (IE er.	EE802.3) in Eth	ernet LAN and	or GR4 series used for Primary-Secondary Coupling cap ations than described in the abov	
	when using	this product for	any other applic		ve.
2. Rating 2-1. Operating tempe	rature range	e -55 to	+125°C		
2-2. Part name configered ex.) GR4 42		R7	LB	102 K W01	L
Series Dimen (L×W		•	ire Rated Capa tic voltage	acitance Capacitance Individual tolerance specificatio	•
· ·	, , ,	Characteria	lic voltage		II Style
 Dimension(Dimens	ion (mm)		
	Code	L	Ŵ	Soldering Method	
	42 43	4.5±0.3 4.5±0.4	2.0±0.2 3.2±0.3	reflow reflow	
	43 55	4.5±0.4 5.7±0.4	5.0±0.4	reflow	
 Dimension(1			
	Code Q			ion (mm) .5	
	D			0	
 Temperatur 		stic			
	Code R7			characteristic 7R	
		irm detailed spe		pecification and test methods].	
 Rated volta 		1	T a a ta		
	Code LB			voltage i3kV	
•Capacitanc The first t ex.) In ca	wo digits de se 102.	note significant = 1000pF	figures ; the last	t digit denotes the multiplier of 10) in pF.
•Capacitanc Please		t number list].			
 Individual s 		1			
	Code W01	Base motal al		ntent sion(T) tolerance : +0/-0.3mm)	
	**01	Dase metal ele			
 Packing sty 	le				
	Code			yle	
	L		¢180mm reel	Plastic taping	

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3. I	Part nu	mber list								
			0.3 min. g mi	n. 0.3 min.	• •					
			L					l	Jnit :	mm
то	Сар.		Outstansen Deut Number	Murata Dart Nurshar	DC Test		Dimen	sion(mm)		Pack
T.C.	(pF)	Cap. Tol.	Customer Part Number	Murata Part Number	Volt. (V)	L	W	т	g	Qty. (pcs
X7R	100	±10 %		GR442QR7LB101KW01L	3000	4.5 ±0.3	2.0 ±0.2	1.5 +0/-0.3	2.5	2000
X7R	120	±10 %		GR442QR7LB121KW01L	3000	4.5 ±0.3	2.0 ±0.2	1.5 +0/-0.3	2.5	2000
X7R	150	±10 %		GR442QR7LB151KW01L	3000	4.5 ±0.3	2.0 ±0.2	1.5 +0/-0.3	2.5	2000
X7R	180	±10 %		GR442QR7LB181KW01L	3000	4.5 ±0.3	2.0 ±0.2	1.5 +0/-0.3	2.5	2000
X7R	220	±10 %		GR442QR7LB221KW01L	3000	4.5 ±0.3	2.0 ±0.2	1.5 +0/-0.3	2.5	2000
X7R	270	±10 %		GR442QR7LB271KW01L	3000	4.5 ±0.3	2.0 ±0.2	1.5 +0/-0.3	2.5	2000
X7R	330	±10 %		GR442QR7LB331KW01L	3000	4.5 ±0.3	2.0 ±0.2	1.5 +0/-0.3	2.5	2000
X7R	390	±10 %		GR442QR7LB391KW01L	3000	4.5 ±0.3	2.0 ±0.2	1.5 +0/-0.3	2.5	2000
X7R	470	±10 %		GR442QR7LB471KW01L	3000	4.5 ±0.3	2.0 ±0.2	1.5 +0/-0.3	2.5	2000
X7R	560	±10 %		GR442QR7LB561KW01L	3000	4.5 ±0.3	2.0 ±0.2	1.5 +0/-0.3	2.5	2000
X7R	680	±10 %		GR442QR7LB681KW01L	3000	4.5 ±0.3	2.0 ±0.2	1.5 +0/-0.3	2.5	2000
X7R	820	±10 %		GR442QR7LB821KW01L	3000	4.5 ±0.3	2.0 ±0.2	1.5 +0/-0.3	2.5	2000
X7R	1000	±10 %		GR442QR7LB102KW01L	3000	4.5 ±0.3	2.0 ±0.2	1.5 +0/-0.3	2.5	2000
X7R	1200	±10 %		GR442QR7LB122KW01L	3000	4.5 ±0.3	2.0 ±0.2	1.5 +0/-0.3	2.5	2000
X7R	1500	±10 %		GR442QR7LB152KW01L	3000	4.5 ±0.3	2.0 ±0.2	1.5 +0/-0.3	2.5	2000
X7R	1800	±10 %		GR443QR7LB182KW01L	3000	4.5 ±0.4	3.2 ±0.3	1.5 +0/-0.3	2.5	1000
X7R	2200	±10 %		GR443QR7LB222KW01L	3000	4.5 ±0.4	3.2 ±0.3	1.5 +0/-0.3	2.5	1000
X7R	2700	±10 %		GR443QR7LB272KW01L	3000	4.5 ±0.4	3.2 ±0.3	1.5 +0/-0.3	2.5	1000

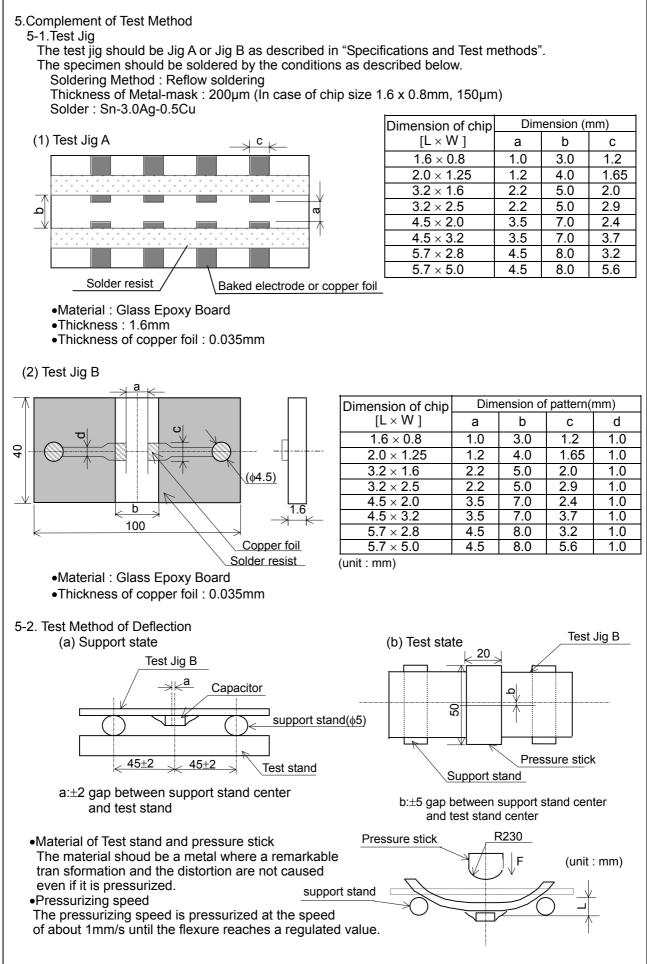
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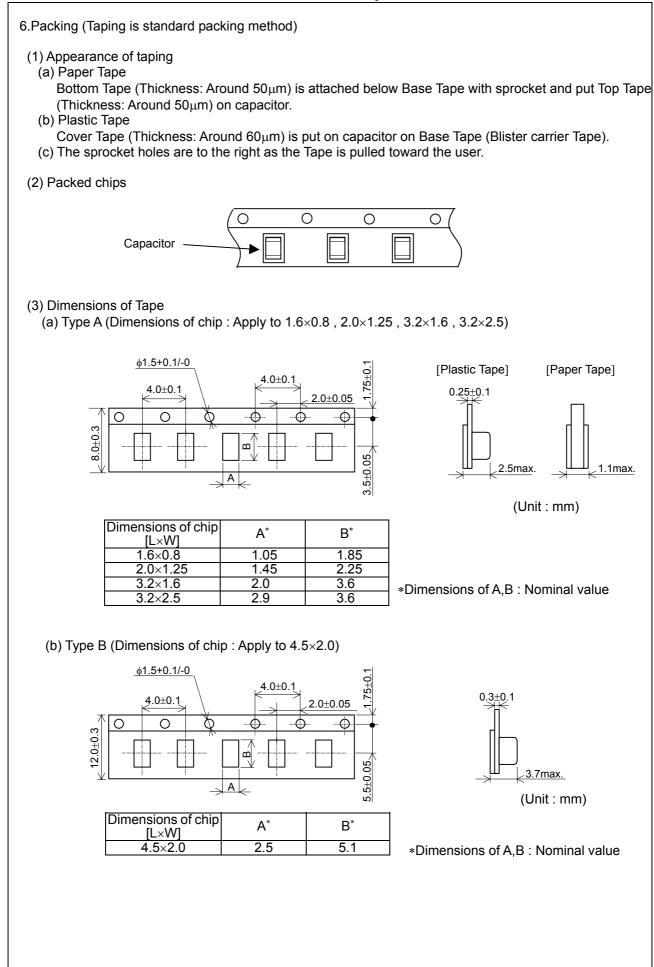
1 0	nocifications and	I toot mothoda						
<u>4. S</u> No.	pecifications and Ite		Specificat	ion		Test met	hod	
				1011		iest met	nou	
1	Operating temper	aluie	-55~+125°C	na aliti				
	Appearance		No defects or abnor		Visual inspection	on.		
3	Dimensions		Within the specified		Using calipers.			
4	Dielectric strength	1	No defects or abnor		DC30	between tharge/disc	the termin	ations,
5	Pulse voltage		No self healing brea	k downs or	10 impulse of a	alternating	polarity is	
-			flash-orvers have ta the capacitor.	ken place in	subjected. (5 in The interval be Applied Pulse : Applied Voltage	npulse for tween imp 1.2/50μs e: 2.5kV₀-r	each pola oulse is 60	arity) Is.
6	Insulation resistar	nce(I.R.)	6000 MΩ or more	,	The insulation with DC500±50 charging.	resistance)V and with	shall be r nin 60±5s	neasured of
7	Capacitance		Within the specified	tolerance.	The capacitance	e/D.F. sha	II be mea	sured at
8	Dissipation Factor	r (D.F.)	0.025 max.		the frequency of AC1±0.2V(r.m.		z and a v	oltage of
9	Capacitance Temperature Cha	racteristics	Cap. change within ±15% (Temp. Range : -5	5 to +125°C)	The capacitance made at each se Pretreatment Perform the he for 60±5 min ar room condition	step specif at treatme nd then let	ïed in tab nt at 150-	le. ⊦0/-10°C
			Г	Cton	1 2	3	4	5
			-	Step Temp.(°C) 2	1 2 25±2 -55±3	3 25±2	4 125±2	5 25±2
			L			2022	12022	2022
	Vibration resistance	Appearance Capacitance D.F.	No defects or abnor Within the specified Pass the item No.8.	tolerance.	Solder the capa epoxy board)sh method". The capacitor s harmonic motic 1.5mm, the free between the ap 55Hz. The frequency return to 10Hz, approximately This motion sha in each of 3 mu (total of 6 h).	nown in "C shall be su on having a quency be oproximate range, fron shall be tr 1 min. all be appli utually perp	bjected to a total am ing varied limits of m 10 to 5 aversed i ed for a p pendicula	ent of test o a simple plitude of uniformly 10 and 5Hz and n eriod of 2 h r directions
	Solderability of termination		75% of the terminat		235±5°C H60A	8101) and veight pro der solutio peed : 25 <u>+</u> r :	rosin (JIS portion). n for 2±0. :2.5mm/s er (Sn-3.0	8 K 5902) 5s. 0Ag-0.5Cu)
12	Resistance to	Appearance	No marking defects.		Preheat	e ·		
	soldering heat	Capacitance	Within ±10%		$LW \le 3.2 \times 1.$	6 : to 150°C fe	or 1 min	
		change	Doop the Harry Mar C		LW ≥3.2 x 1.6			
		D.F.	Pass the item No.8.			5 . to 120°C fo	or 1 min o	nd then
		I.R. Dialantria	1000 M Ω or more			to 200°C f		
		Dielectric strength	Pass the item No.4.		Immerse the ca 260±5°C for 10 Let sit at room measure. Immersing in s •Pretreatment Perform the he for 60±5 min ar room condition	apacitor in)±1s. condition* peed : 25± at treatme nd then let	solder so for 24±2 :2.5mm/s. nt at 150-	h, then ⊦0/-10°C

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Reference on	V
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15 Temperature cycle Appearance No marking defects. Fix the capacitor to the supporting Test Jig A (diss epoxy board) shown in "Complement of test method". 15 Temperature cycle Appearance No marking defects. Fix the capacitor to the supporting Test Jig A (diss epoxy board) shown in "Complement of test method". 16 J.F. 0.05 max. Perform the 5 cycles according to the 4 heat treatments listed the following table. 16 Humidity Appearance No marking defects. 17 Life Appearance No marking defects. 18 Humidity Appearance No marking defects. 19 Life Appearance No marking defects. 10 D.F. 0.05 max. Sitt the capacitor at 40±2°C and relative humidity 90 to 95% for 500+24/-0 h. 17 Life Appearance No marking defects. Pretreatment for 60±5 min and then let sit for 24±2 h at room condition*. 17 Life Appearance No marking defects. Apply DC2.2KV for 1000+48/-0 h. 18 Appearance No marking defects. Apply DC2.2KV for 1000+48/-0 h at maximun con	15 Temperature cycle Appearance No marking defects. Fix the capacitor to the supporting Test Jig (Capacitance change 15 Temperature cycle Appearance No marking defects. Fix the capacitor to the supporting Test Jig (Capacitance change 16 I.R. 3000 MΩ or more Perform the 5 cycles according to the 4 he reatments listed the following table. 16 Humidity Appearance No marking defects. 17 Life Appearance No marking defects. 17 Life Appearance No marking defects. 17 Life Appearance No marking defects. 18 Appearance No marking defects. Sit the capacitor at 40±2°C and relative humidity 90 to 95% for 500+24/-0 h. 17 Life Appearance No marking defects. Appearance 17 Life Appearance No marking defects. Appearance 18 Appearance No marking defects. Apple DC2 2K/ tor 1000+48/-0 h at maximu condition*. 17 Life Appearance No marking defects. Apply DC2 2K/ tor 100	15 Temperature cycle Appearance No marking defects. Fix the of test in + Flexu + Hold is + Flexu + Hold is + Hold is + Flexu + Fle	Test Method of Deflection" of "Complement test method". Flexure : 1mm Hold time : 5s x the capacitor to the supporting Test Jig A lass epoxy board) shown in "Complement test method". erform the 5 cycles according to the 4 heat eatments listed the following table. $\frac{$ Step $ Temp. (°C) $ Time (min)$}{1$ -55\pm3$ 30\pm3$} $ \frac{30\pm3}{2$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm2$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm2$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm2$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm2$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm2$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm2$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm2$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm2$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm2$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm2$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm2$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm2$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm2$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm2$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm2$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm2$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm2$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm2$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm2$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm2$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm2$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm2$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm2$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm2$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm2$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm3$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm3$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm3$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm3$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm3$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm3$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm3$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm3$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm3$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm3$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm3$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm3$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ \frac{3$ 125\pm3$ 30\pm3$}{4$ Room Temp. 2 to 3$} $ 3$ 125\pm3$
15 Temperature cycle Appearance No marking defects. Fix the capacitor to the supporting Test Jig A (glass epoxy board) shown in "Complement of test method". 15 Temperature change D.F. 0.05 max. Perform the 5 cycles according to the 4 heat treatments listed the following table. 17 D.F. 0.05 max. Step Temp. (*C) Time (min) 1 - 5543 18 Dielectric strength Pass the item No.4. Step Temp. (*C) Time (min) 1 - 5543 16 Humidity (Steady state) Appearance change No marking defects. Sit the capacitor at 0+2°C and relative for 60±5 min and then let sit for 24±2 h at room condition*. 16 Humidity (Steady state) Appearance change No marking defects. Sit the capacitor at 40±2°C and relative humidity 90 to 95% for 500+24/-0 h. 17 Life Appearance change No marking defects. Sit the capacitor at 40±2°C and relative humidity 90 to 95% for 500+24/-0 h. 17 Life Appearance change No marking defects. Cordition, then measure. 17 Life Appearance change No marking defects. Apply DC2.2XV for 1000+48/-0 h at maximun operating temperature±3°C. 17 Life Appearance change No marking defects. Apply DC2.2XV for 1000+48/-0 h at maximun operating temperature±3°C. 17 Life Appearance change No marking defects.<	15 Temperature cycle Appearance Capacitance change No marking defects. Fix the capacitor to the supporting Test Jig (glass epoxy board) shown in "Complement of test method". 15 Temperature cycle Appearance Within ±15% (glass epoxy board) shown in "Complement of test method". 16 D.F. 0.05 max. Perform the 5 cycles according to the 4 he treatments listed the following table. 17 Life Appearance change No marking defects. Sit the capacitor to more of test method". 16 Humidity (Steady state) Appearance capacitance change No marking defects. Sit the capacitor at 40±2°C and relative nor condition*. 16 Humidity (Steady state) Appearance capacitance change No marking defects. Sit the capacitor at 40±2°C and relative numidity 90 59% for 500±24/-0 h. Remove and let sit for 24±2 h at "room condition." 17 Life Appearance change No marking defects. of for 60±5 min and then let sit for 24±2 h at room condition*. 17 Life Appearance change No marking defects. Apply DC2.2kV for 1000+48/-0 h at maximu operating temperature±3°C. Remove and let sit for 24±2 h at "room condition, then measure. 17 Life Appearance change No marking defects. Apply DC2.2kV for 1000+48/-0 h at maximu operating temperature±3°C. Remove and let sit for 24±2 h at "room condition, then measure. 17 Life Appearance change <th>15 Temperature cycle Appearance No marking defects. Fix the or class of test in + Flexu + Hold in + Hold</th> <th>test method". Flexure : 1mm Hold time : 5s x the capacitor to the supporting Test Jig A lass epoxy board) shown in "Complement test method". erform the 5 cycles according to the 4 heat eatments listed the following table. $\frac{\$ \text{Step} \text{Temp. (°C)} \text{Time (min)}}{1 -55\pm 3 30\pm 3} \\ \hline 2 \text{Room Temp. } 2 \text{ to } 3 \\ \hline 3 125\pm 2 30\pm 3} \\ \hline 4 \text{Room Temp. } 2 \text{ to } 3 \\ \hline 4 \text{Room Temp. } 2 \text{ to } 3 \\ \hline 4 \text{Room Temp. } 2 \text{ to } 3 \\ \hline 4 \text{Room Temp. } 2 \text{ to } 3 \\ \hline 4 \text{Room Temp. } 2 \text{ to } 3 \\ \hline 4 \text{Room Temp. } 2 \text{ to } 3 \\ \hline 4 \text{Room Temp. } 2 \text{ to } 3 \\ \hline 4 \text{Room Temp. } 2 \text{ to } 3 \\ \hline 4 \text{Room Temp. } 2 \text{ to } 3 \\ \hline 4 \text{Room Temp. } 2 \text{ to } 3 \\ \hline 4 \text{Room Temp. } 2 \text{ to } 3 \\ \hline 4 \text{Room Temp. } 2 \text{ to } 3 \\ \hline 4 \text{Room Temp. } 2 \text{ to } 3 \\ \hline 5 10000000000000000000000000000000000$</th>	15 Temperature cycle Appearance No marking defects. Fix the or class of test in + Flexu + Hold in + Hold	test method". Flexure : 1mm Hold time : 5s x the capacitor to the supporting Test Jig A lass epoxy board) shown in "Complement test method". erform the 5 cycles according to the 4 heat eatments listed the following table. $\frac{$ \text{Step} \text{Temp. (°C)} \text{Time (min)}}{1 -55\pm 3 30\pm 3} \\ \hline 2 \text{Room Temp. } 2 \text{ to } 3 \\ \hline 3 125\pm 2 30\pm 3} \\ \hline 4 \text{Room Temp. } 2 \text{ to } 3 \\ \hline 4 \text{Room Temp. } 2 \text{ to } 3 \\ \hline 4 \text{Room Temp. } 2 \text{ to } 3 \\ \hline 4 \text{Room Temp. } 2 \text{ to } 3 \\ \hline 4 \text{Room Temp. } 2 \text{ to } 3 \\ \hline 4 \text{Room Temp. } 2 \text{ to } 3 \\ \hline 4 \text{Room Temp. } 2 \text{ to } 3 \\ \hline 4 \text{Room Temp. } 2 \text{ to } 3 \\ \hline 4 \text{Room Temp. } 2 \text{ to } 3 \\ \hline 4 \text{Room Temp. } 2 \text{ to } 3 \\ \hline 4 \text{Room Temp. } 2 \text{ to } 3 \\ \hline 4 \text{Room Temp. } 2 \text{ to } 3 \\ \hline 4 \text{Room Temp. } 2 \text{ to } 3 \\ \hline 5 10000000000000000000000000000000000$
15 Temperature cycle Appearance No marking defects. Fix the capacitor to the supporting Test Jig A (Jass epoxy board) shown in "Complement of test method". 15 Temperature cycle D.F. 0.05 max. Fix the capacitor to the supporting Test Jig A (Jass epoxy board) shown in "Complement of test method". 16 D.F. 0.05 max. Perform the 5 cycles according to the 4 heat treatments listed the following table. 16 Humidity. Appearance No marking defects. Step Temp. (*C) Time (min) 16 Humidity. Appearance No marking defects. Stit the capacitor at 40±2°C and relative humidity 90 to 95% for 500+24/-0 h. 17 Life Appearance No marking defects. Stit the capacitor at 40±2°C and relative humidity 90 to 95% for 500+24/-0 h. 17 Life Appearance No marking defects. condition*. 17 Life Appearance No marking defects. condition*. 17 Life Appearance No marking defects. condition*. 18 Mapearance No marking defects. condition*. 19 Life Appearance No marking defects. condition*. 18 1000 MΩ or more <th>15 Temperature cycle Appearance No marking defects. Fix the capacitor to the supporting Test Jig (gass epoxy board) shown in "Complemer of test method". 15 Temperature cycle Within ±15% (glass epoxy board) shown in "Complemer of test method". 16 D.F. 0.05 max. Perform the 5 cycles according to the 4 he treatments listed the following table. 17 Life Appearance No marking defects. Site nemp. (°C) Time (min) 18 Jielectric Pass the item No.4. Site nemp. (°C) Time (min) 19 Appearance No marking defects. No marking defects. Perform the heat treatment at 150+0/-10°C for 60±5 min and then let sit for 24±2 h at room condition*, then measure. 16 Humidity Appearance No marking defects. Sit the capacitor at 40±2°C and relative humidity 90 to 95% for 500+24/-0 h. 17 Life Appearance No marking defects. Perform the heat treatment at 150+0/-10°C for 60±5 min and then let sit for 24±2 h at "room condition*. 17 Life Appearance No marking defects. Apply DC2.2kV for 1000+48/-0 h at maximu operating temperature4.3°C. 17 Life Appearance No marking defects. Apply DC2.2kV for 1000+48/-0 h at maximu operating temperature4.3°C.<th>15 Temperature cycle Appearance No marking defects. Fix the original system of test in the ori</th><th>Flexure : 1mm Hold time : 5s x the capacitor to the supporting Test Jig A lass epoxy board) shown in "Complement test method". erform the 5 cycles according to the 4 heat eatments listed the following table.</th></th>	15 Temperature cycle Appearance No marking defects. Fix the capacitor to the supporting Test Jig (gass epoxy board) shown in "Complemer of test method". 15 Temperature cycle Within ±15% (glass epoxy board) shown in "Complemer of test method". 16 D.F. 0.05 max. Perform the 5 cycles according to the 4 he treatments listed the following table. 17 Life Appearance No marking defects. Site nemp. (°C) Time (min) 18 Jielectric Pass the item No.4. Site nemp. (°C) Time (min) 19 Appearance No marking defects. No marking defects. Perform the heat treatment at 150+0/-10°C for 60±5 min and then let sit for 24±2 h at room condition*, then measure. 16 Humidity Appearance No marking defects. Sit the capacitor at 40±2°C and relative humidity 90 to 95% for 500+24/-0 h. 17 Life Appearance No marking defects. Perform the heat treatment at 150+0/-10°C for 60±5 min and then let sit for 24±2 h at "room condition*. 17 Life Appearance No marking defects. Apply DC2.2kV for 1000+48/-0 h at maximu operating temperature4.3°C. 17 Life Appearance No marking defects. Apply DC2.2kV for 1000+48/-0 h at maximu operating temperature4.3°C. <th>15 Temperature cycle Appearance No marking defects. Fix the original system of test in the ori</th> <th>Flexure : 1mm Hold time : 5s x the capacitor to the supporting Test Jig A lass epoxy board) shown in "Complement test method". erform the 5 cycles according to the 4 heat eatments listed the following table.</th>	15 Temperature cycle Appearance No marking defects. Fix the original system of test in the ori	Flexure : 1mm Hold time : 5s x the capacitor to the supporting Test Jig A lass epoxy board) shown in "Complement test method". erform the 5 cycles according to the 4 heat eatments listed the following table.
15 Temperature cycle Appearance No marking defects. Fix the capacitor to the supporting Test Ig A (glass epoxy board) shown in "Complement of test method". 17. D.F. 0.05 max. Perform the 5 cycles according to the 4 heat treatments listed the following table. 18. 3000 MΩ or more Dielectric Pass the item No.4. 19. Exercise according to the 4 heat treatments listed the following table. Step Temp. ("C) Time (min) 1 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (30±3) (4 (-55±3) (4 (-55±3) (4 (-55±3) (4 (-55±3) (4 (-55±3) (4 (-55±3) (4 (-55±3) (4 (-55±3) (4 (-55±3) (4 (-55±3) (4 (-55±3) (4 (-55±3) (4 (-55±3) (4 (-55±3) (4 (-55±3) (4 (-55±3) (4 (-55±3) (4 (-55±3) (4 (-55±3) (4 (-55±3) (4 (-55±3) (4 (-55±3) (4 (-55±3) (4 (-55±3) (4 (-55±3) (4 (-55±3) (4 (-55±3) (4 (-55±3) (4 (-55±3) (4 (-55±3) (4 (-55±3) (4 (-55±3	15 Temperature cycle Appearance No marking defects. Fix the capacitor to the supporting Test Jig (glass epoxy board) shown in "Complement of test method". 16 D.F. 0.05 max. Perform the 5 cycles according to the 4 he following table. 17 Dielectric Pass the item No.4. Step Temp. (*C) Time (min). 16 Humidity Appearance No marking defects. Site of test method". 16 Humidity Appearance No marking defects. Site of test method". 16 Humidity Appearance No marking defects. Site of 24±2 h at room condition*, then measure. 16 Humidity Appearance No marking defects. Sit the capacitor at 40±2°C and relative for 60±2 hor. 17 Life Appearance No marking defects. Sit the capacitor at 40±2°C and relative for 60±2 hor. 18 Humidity Appearance No marking defects. Sit the capacitor at 40±2°C and relative for 60±5 min and then let sit for 24±2 h at "room condition". 17 Life Appearance No marking defects. Perform the heat treatment at 150+0/-10°C for 60±2 min and then let sit for 24±2 h at "room condition". 17 Life Appearance No marking defects. Perform	15 Temperature cycle Appearance No marking defects. Fix the original system of test in the ori	Hold time : 5sx the capacitor to the supporting Test Jig A lass epoxy board) shown in "Complement itest method".endine to the supporting to the 4 heat eatments listed the following table.StepTemp. (°C)1 -55 ± 3 2Room Temp.2to 33 125 ± 2 30\pm3 4 4Room Temp.2to 3easure.2Pretreatment
15 Temperature cycle Appearance No marking defects. Fix the capacitor to the supporting Test Jig A (glass epoxy board) shown in "Complement of test method". D.F. 0.05 max. Perform the 5 cycles according to the 4 heat treatments listed the following table. Dielectric Pass the item No.4. Step Temp. (*C) Time (min) 14 -55±3 3043 2 Room Temp. 2 to 3 2 Room Temp. 2 to 3 3 125±2 30±3 2 Room Temp. 2 to 3 4 Room Temp. 2 to 3 16 Humidity Appearance No marking defects. Sit the capacitor at 40±2°C and relative nom condition*, then measure. 16 Humidity Appearance No marking defects. Sit the capacitor at 40±2°C and relative nom condition*. 17 Life Appearance No marking defects. Sit the capacitor at 40±2°C and relative nom condition*. 17 Life Appearance No marking defects. Perform the heat treatment at 150+0/-10°C for 60±5 min and then let sit for 24±2 h at "room condition. 17 Life Appearance No marking defects. Perform the heat treatment at 150+0/-10°C for 60±5 min and then let sit for 24±2 h at "room condition.	15 Temperature cycle Appearance Capacitance (hange D.F. 0.05 max. Dielectric strength) Fit the capacitor to the supporting Test Jig (glass epoxy board) shown in "Complemer of test method". 16 I.R. 3000 MΩ or more Dielectric Pass the item No.4. Perform the 5 cycles according to the 4 he treatments listed the following table. 16 Humidity (Steady state) Appearance No marking defects. Capacitance of test method". Sten Temp. (*C) Time (min). 16 Humidity (Steady state) Appearance No marking defects. Capacitance of test is for 24±2 h at room condition*. Stif the capacitor at 40±2°C and relative nor condition*. 17 Life Appearance No marking defects. Capacitance of test is the 200 MΩ or more treatment at 150+0/-10°C for 60±5 min and then let sit for 24±2 h at room condition*. 17 Life Appearance No marking defects. Capacitance of the strength No marking defects. Capacitance of test strength 17 Life Appearance No marking defects. Capacitance of test strength Perform the heat treatment at 150+0/-10°C for 60±5 min and then let sit for 24±2 h at room condition*. 17 Life Appearance No marking defects. Or more D.F. 0.05 max. Capacitance of test method. Perform the heat reatment at 150+0/-10°C for 60±5 min and then let sit for 24±2 h at room condition. 17 Life Appearance No marking defects. Dielectric Pass the item No.4. Strength Apply DC2.2kV for	15 Temperature cycle Appearance No marking defects. Fix the original system of test in the ori	x the capacitor to the supporting Test Jig A lass epoxy board) shown in "Complement test method". erform the 5 cycles according to the 4 heat eatments listed the following table. $\begin{array}{ c c c c c c c c c c c c c c c c c c c$
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Reference only

